

(12) UK Patent Application (19) GB (11) 2 171 876 A

(43) Application published 3 Sep 1986

(21) Application No 8604371

(22) Date of filing 21 Feb 1986

(30) Priority data

(31) 74419

(32) 22 Feb 1985

(33) IL

(51) INT CL⁴
H05K 3/00

(52) Domestic classification
(Edition H)
H4F EL S24 S25R S30K S30X S42M
U1S 2087 H4F

(56) Documents cited
GB A 2033307 GB A 2020520 EP A2 0120387
WO A1 83/02179

(58) Field of search
H4F G2A H4T
Selected US specifications from IPC sub-classes H04N H05K

(71) Applicants

Optrotech Ltd (Israel)
P O Box 69, Nes Ziona 70450, Israel

(72) Inventors

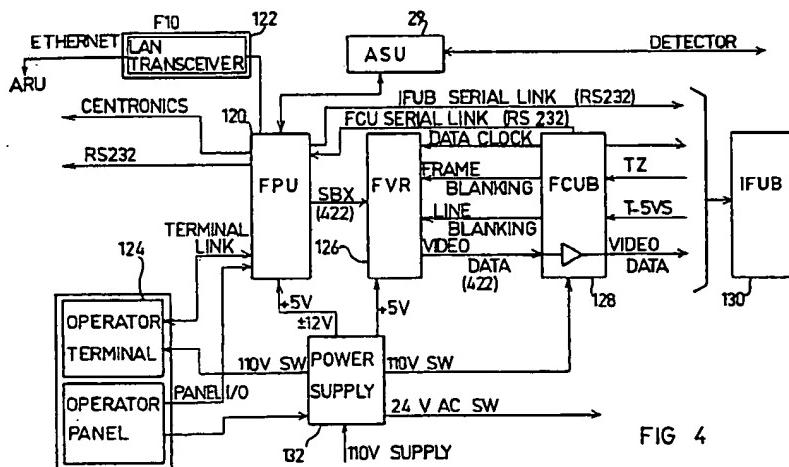
Michael Brunstein
Gershon Miller
Moshe Kovarsky

(74) Agent and/or Address for Service

Marks & Clerk, 57-60 Lincoln's Inn Fields, London WC2A 3LS

(54) Artwork editing, archiving and production system

(57) Printed circuit board designs are stored in archive unit ARU in vector format and can be read out to a laser plotter (IFUB) 130 with conversion into raster format in converter (FVR) 126.



GB 2 171 876 A

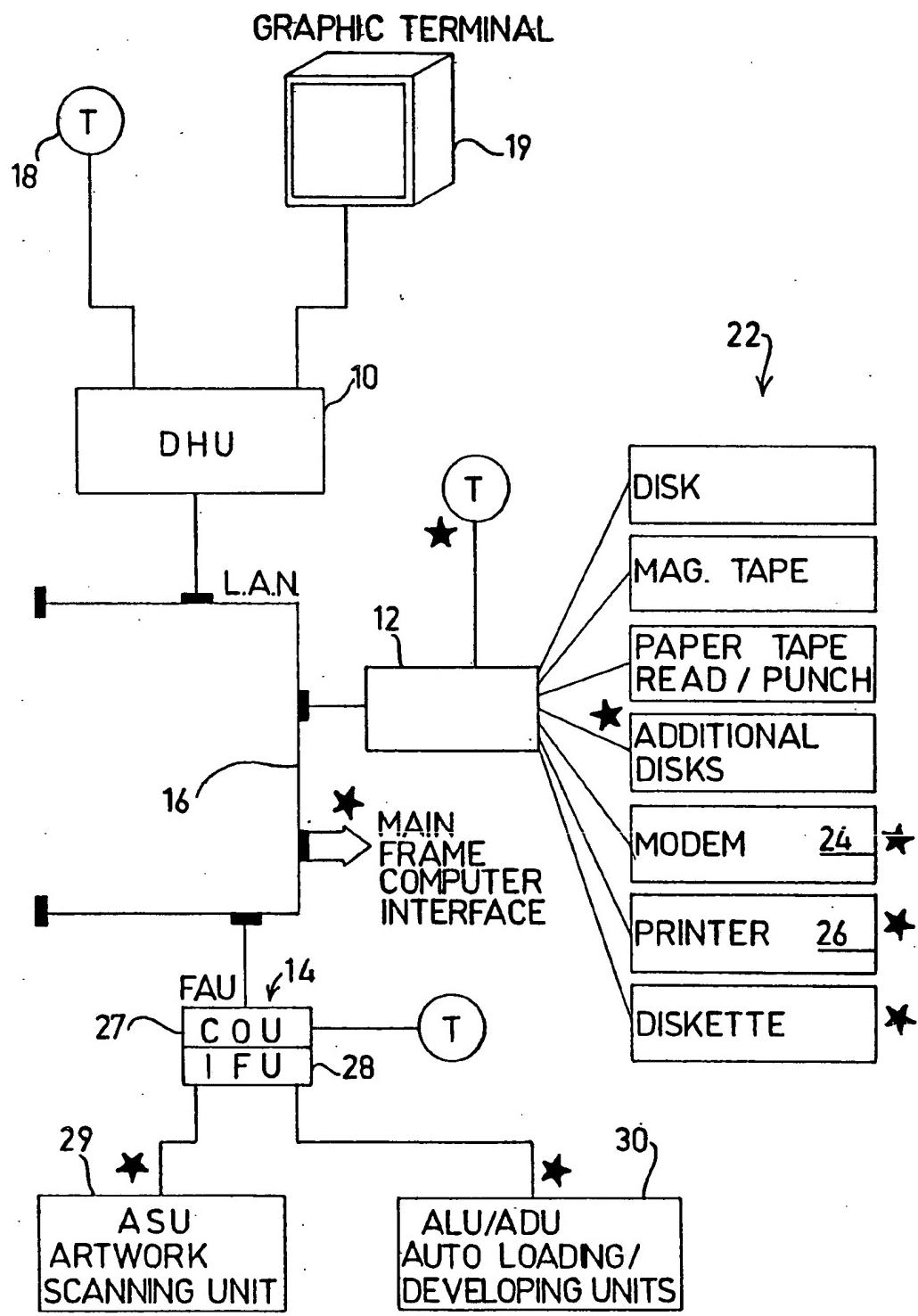


FIG 1

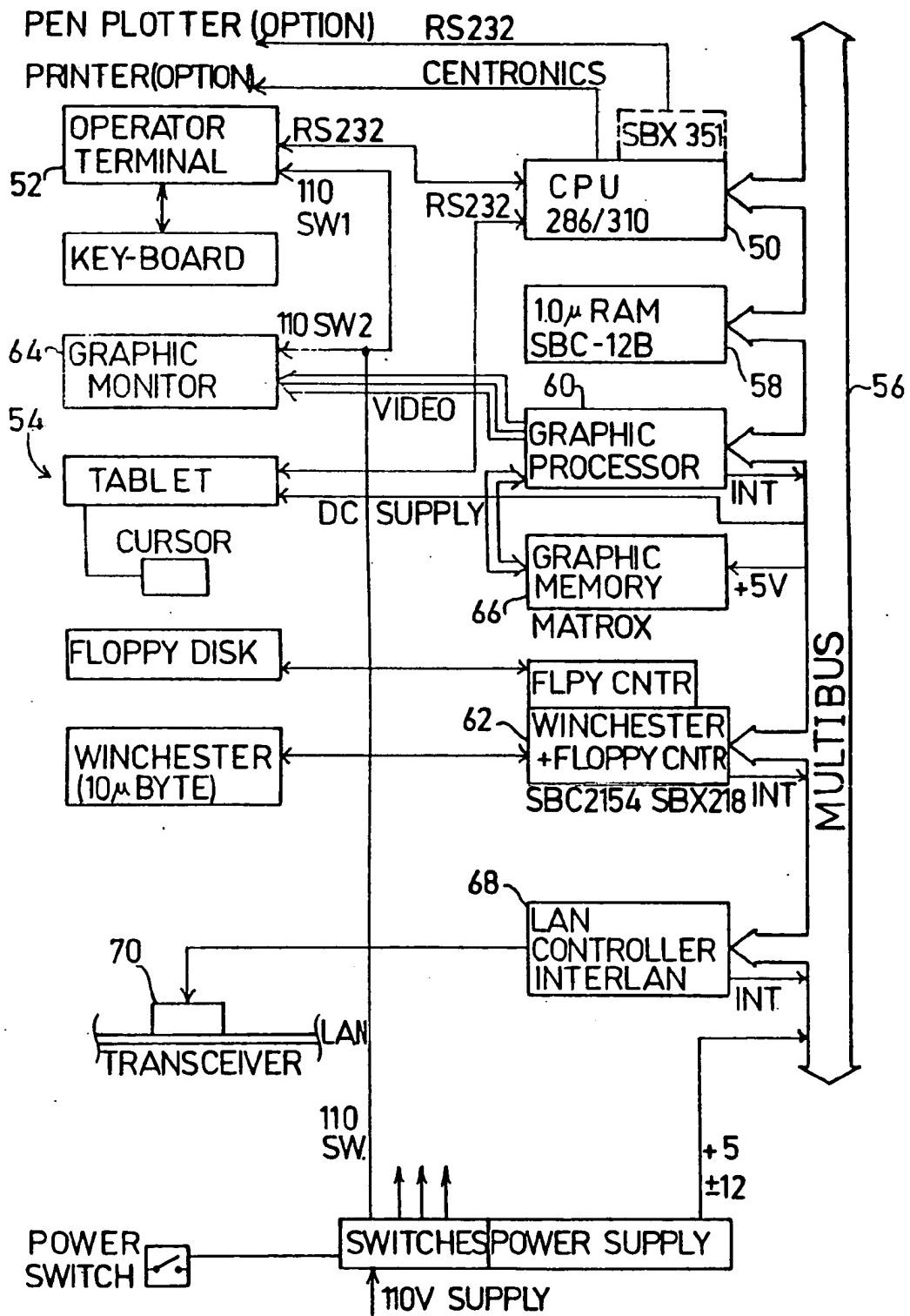


FIG 2

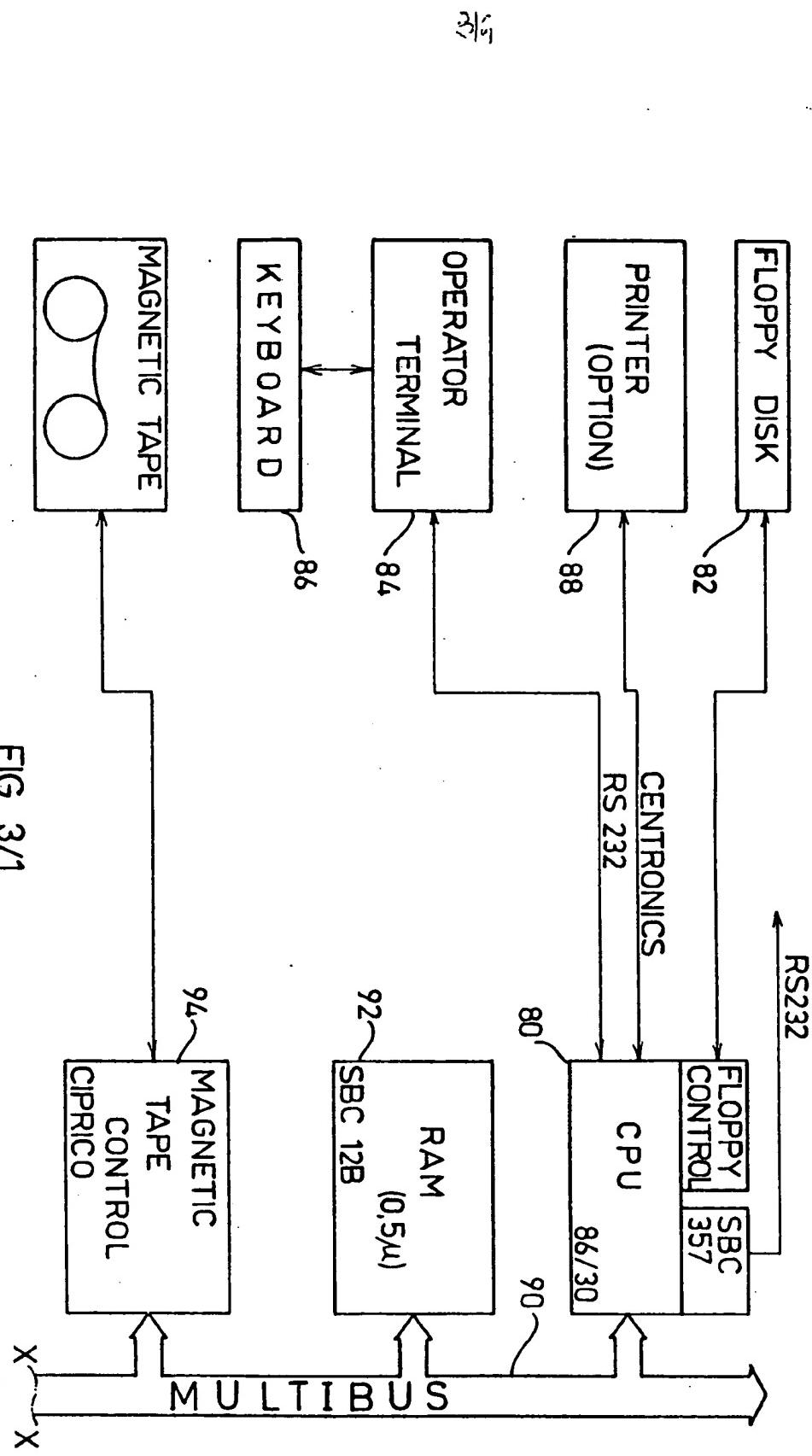


FIG 3/1

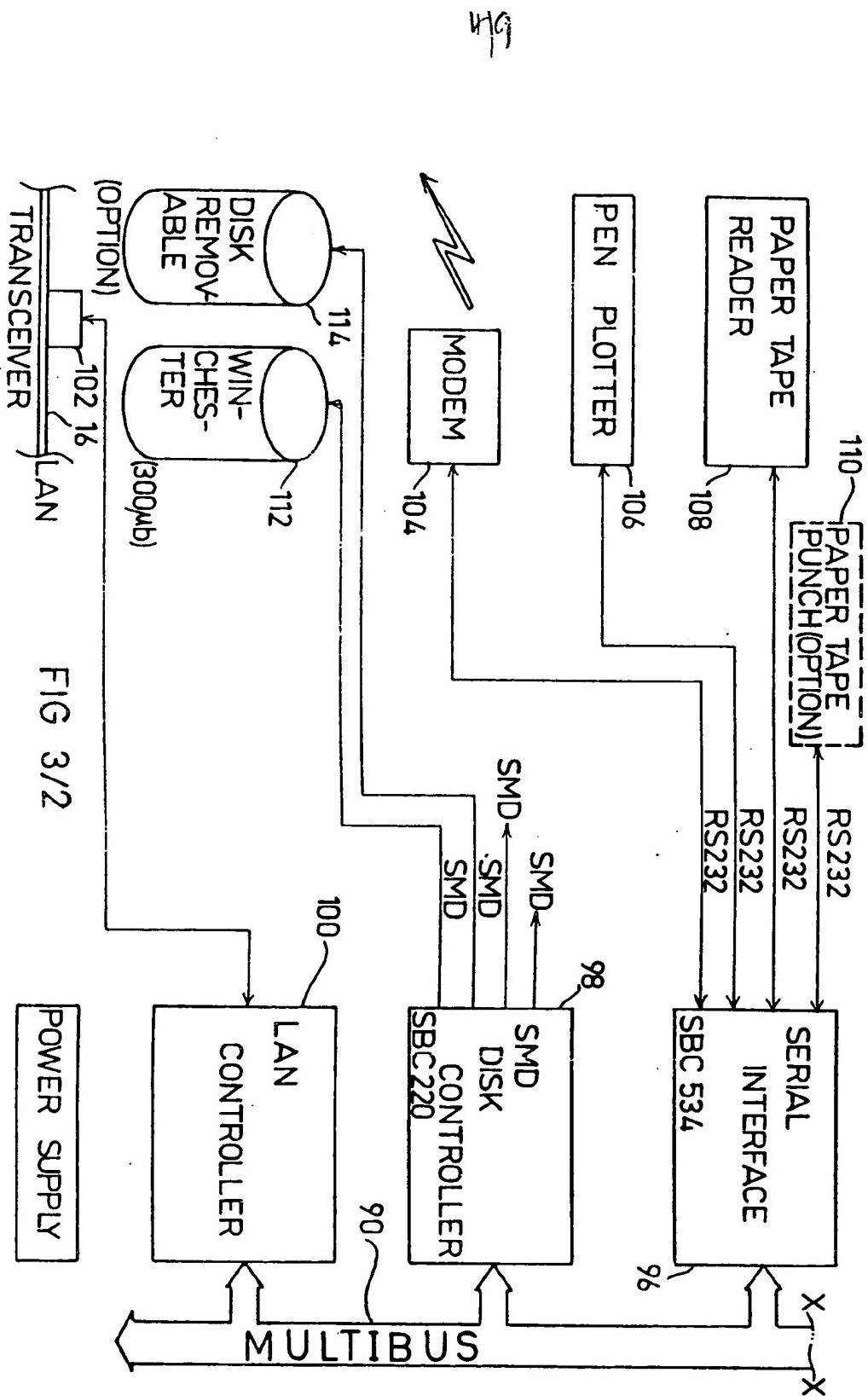


FIG 3/2

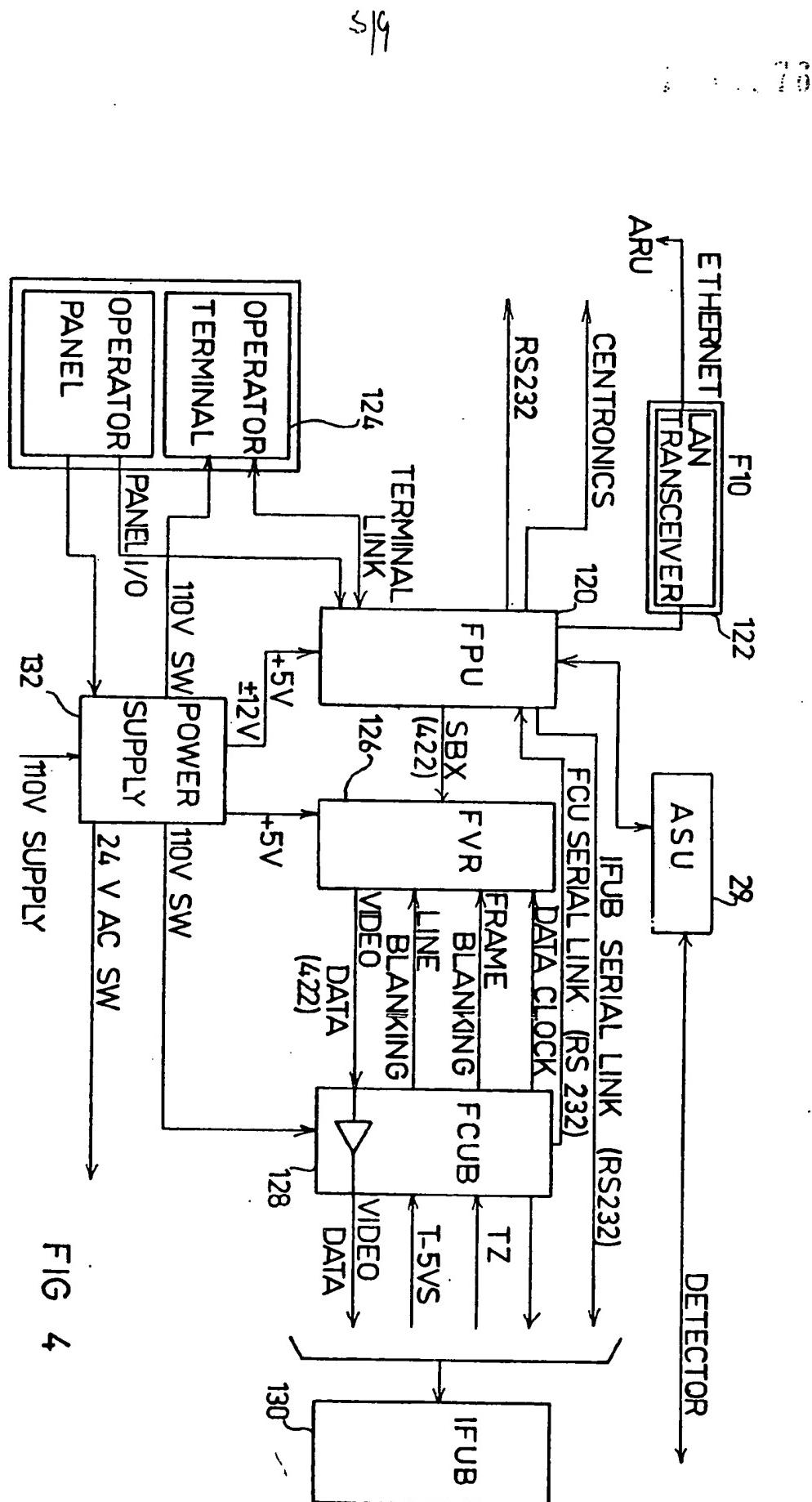


FIG
4

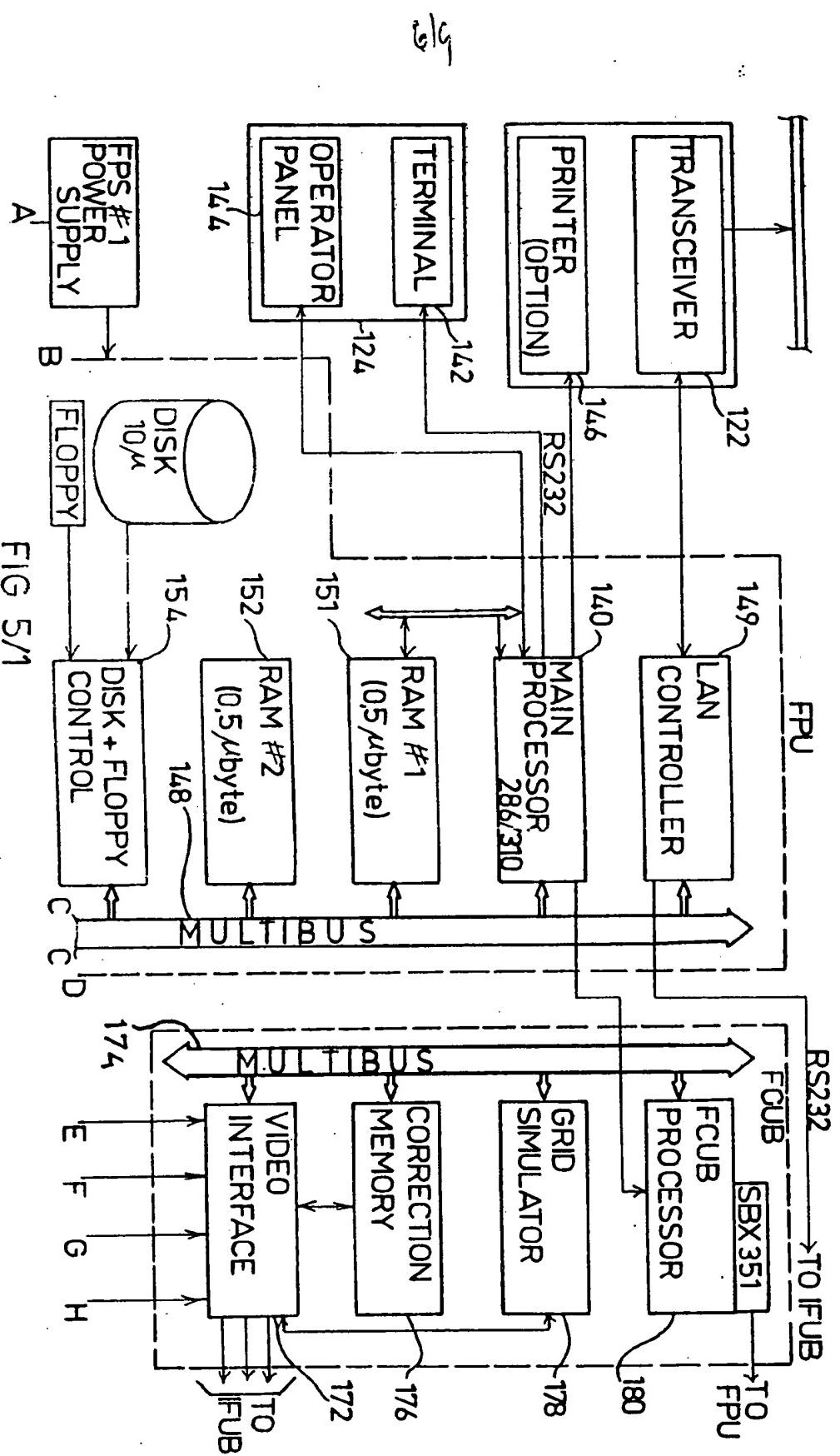


FIG 5/1

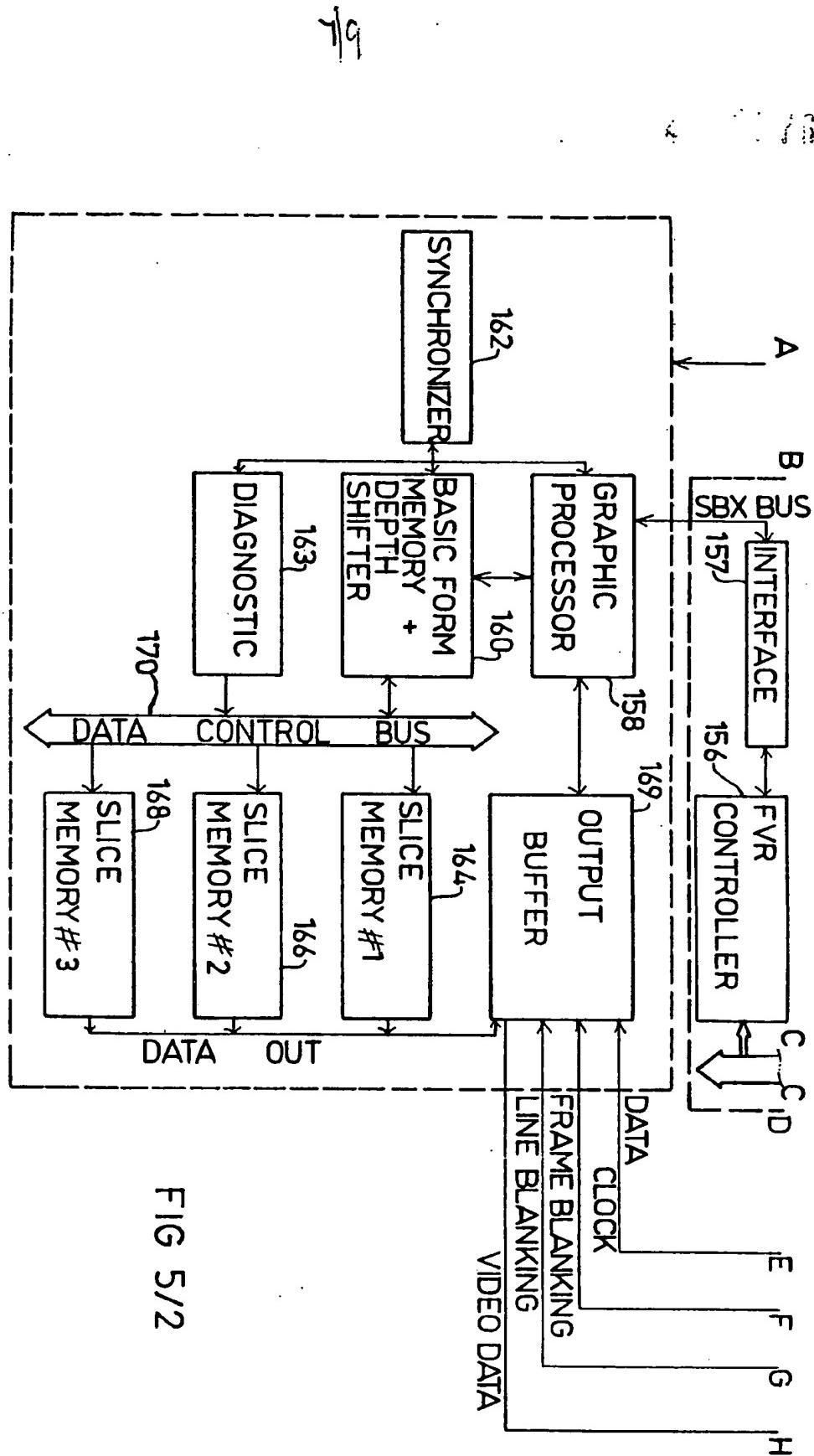


FIG 5/2

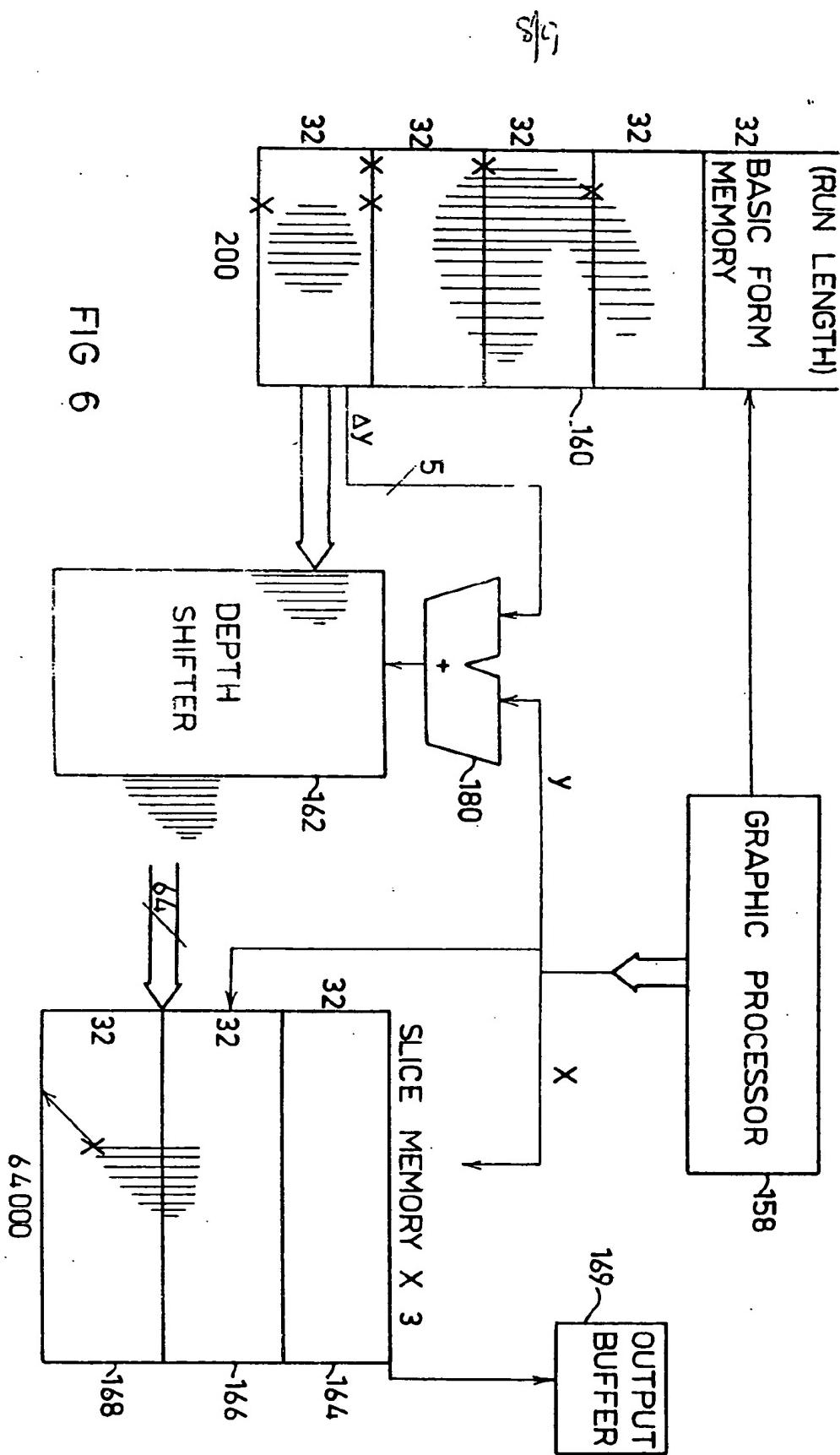


FIG 6

176

90°

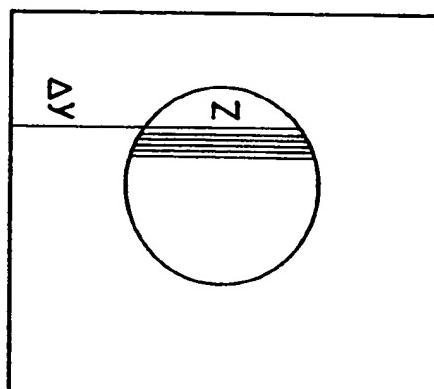


FIG 7

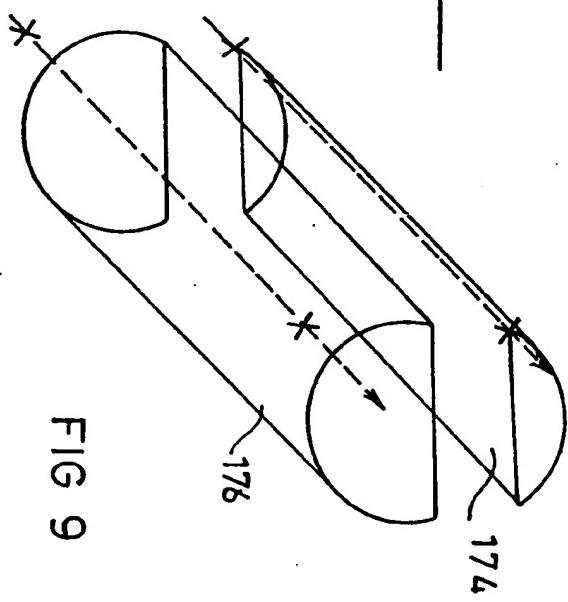


FIG 9

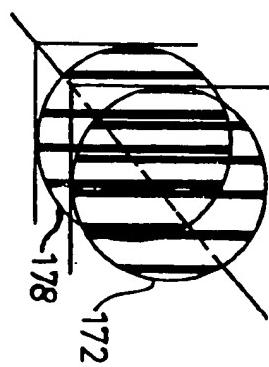


FIG 8

raster conversion apparatus employed in the apparatus show in Fig. 5;

Fig. 7 is an illustration of a typical basic form, useful in understanding the operation of the apparatus

5 illustrated in Fig. 6;

Fig. 8 is a pictorial illustration of a translated basic form used to define a line; and

Fig. 9 is a pictorial illustration of a slice basic form.

DETAILED DESCRIPTION OF THE

10 INVENTION

Reference is now made to Fig. 1 which is a generalized block diagram of the integrated artwork archiving, editing and production system of the present invention. The system includes a data handling unit (D.H.U.) 10, an archive unit (A.R.U.) 12, and a fabrication unit (F.A.U.) 14, all of which interface, preferably via a local area network (LAN) 16, such as as Ethernet, a trademark of Xerox Corporation.

Generally speaking, the data handling unit provides 20 the editing function and interfaces with a terminal 18 such as a conventional computer terminal and a color graphics display 19. The data handling unit, together with its operator interfaces may be understood as being a graphics interactive work station.

25 The electronically edited design produced in the data handling unit 10 is transferred to the archive unit 12 for storage and future use. The archive unit stores a plurality of files, each containing the entire board design including all of the layers, including the solder mask, silk screen mask and drilling design, for a given board. The archive unit can interface with a number of input-output and storage devices 22 such as magnetic tape, punched tape or disk. The archive unit is capable of providing drilling tapes which can be used for 30 automatic processing of the printed circuit boards.

Communication directly with the archive unit may be provided by a modem 24 via a LAN or alternatively directly via an RS 232 serial port. A printer 26 may also be coupled to the archive unit.

40 The data stored in the archive unit can be called up by the fabrication unit for production of the artwork or mask used in exposing the printed circuit board. This artwork is compatible with existing exposure machines.

45 The fabrication unit 14 includes a control and operation unit 27 and an associated image formation unit (IFU) 28, including a laser plotter. Associated therewith are an artwork scanning unit 29 which provides an input by scanning existing artwork and 50 optional auto loading and developing units 30.

Reference is now made to Fig. 2 which is a block diagram illustration of the data handling unit 10. As seen in Fig. 2, the data handling unit comprises a CPU 50 such as an Intel 286/310, which is optionally

55 coupled to a pen plotter (not shown) and a printer (not shown). The CPU 50 is also coupled to an operator terminal and associated keyboard 52 and to a cursor (puck) and tablet device 54, such as a Summographic Bit Pad II.

60 CPU 50 is coupled via a multibus connection 56 to a 1.0 megabyte random access memory 58, a graphic processor and graphic memory 60, such as a Matrox GXB 1000, a disk drive 62, such as a Winchester drive, and local area network 16 (Fig. 1) via a LAN controller 68, such as an Interlan NI 3010, and associated LAN

transceiver 70. Power supplies and connections to the various components are indicated generally in Fig. 2. Graphic processor 60 provides a video output to a high-resolution graphic monitor 64 such as a Barco CDCT 5351 or a Hitachi type HM 3619A.

70 Reference is now made to Fig. 3 which illustrates the archive unit 12 in block diagram form. The archive unit comprises a CPU 80, such as an Intel 86/30, having an associated floppy disk controller and RS 232 serial port. CPU 80 is coupled to a floppy disk drive 82, to an operator terminal 84 and keyboard 86 and may also be coupled to an optional printer 88 of conventional construction.

CPU 80 is coupled via a multibus connection 90 to a 80 0.5 megabyte random access memory 92, a magnetic tape controller 94, such as a Ciprico Tapemaster A. a serial interface 96 having four RS 232 serial ports, an SMD disk controller 98, such as an Intel SBC 220 and local area network 16 (Fig. 1) via a controller 100, such

85 as an Interlan NI 3010 and associated LAN transceiver 102. The RS 232 serial ports of the serial interface 96 may be coupled to a Modem 104, a pen plotter 016, a paper tape reader 108 and a paper tape punch 110 or alternatively to other suitable communications components. The ports of the SMD disk controller 98 are coupled to a hard disk 112 and to an optional removable disk drive 114 and can be coupled to up to four SMD (Standard Module Devices) disks.

90 Reference is now made to Fig. 4 which is a block diagram illustration of the control and operating unit (COU) 27 which forms a part of the fabrication unit 14 (Fig. 1). Generally speaking, the COU receives data from the archive unit 12 and provides an output to a laser plotter forming part of the fabrication unit.

95 The COU comprises a fabrication processor unit (FPU) 120, which interfaces with the ARU via a LAN transceiver 122 and with operator interface apparatus 124. The FPU is operative to receive data from the archive unit to divide it into slices for operation

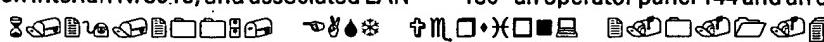
100 thereon by a vector to raster converter 126 (FVR). The vector to raster converter 126 is operative to receive timing signals from, and to provide instruction signals to, a laser plotter interface (FCUB) 128, which, in turn, operates IFUB apparatus 130, which is typically a laser plotter. FCUB circuitry 128 is operative to effect dimensional corrections of the patterns in accordance with instructions received from the main processor

110 140 (Fig. 5). A power supply 132 provides the necessary power requirements of the various components.

115 An artwork scanning unit (ASU) 29 (Fig. 1) may be optionally provided. This unit scans information from artwork in raster form and converts it into vector form for transmittal to the ARU and subsequent storage.

120 This unit may be useful for quickly reading into the ARU information regarding a circuit pattern, which is physically available but not present in vector form in the ARU. The ASU is not required for system performance.

125 Reference is now made to Fig. 5 which shows the FPU, FVR and FCUB of Fig. 4 in more detail. As seen in Fig. 5, the FPU comprises a main processor 140, typically an Intel 286/310, which interfaces with an operator interface 124 (Fig. 4) including a terminal 142, 130 an operator panel 144 and an optional printer 146.



Main processor 140 is operative to convert the full board image of a typical size of 48,000 pixels x 60,000 pixels in vector form, into slices, each typically of size 32 pixels x up to 48,000 pixels. Each pixel corresponds 5 to an area of 0.0005 inch x 0.0005 inch.

Main processor 140 communicates via a multibus 148 with a LAN transceiver 122 via a LAN controller 149, typically an Interlan NI 3010, a pair of 0.5 megabyte RAMs 151 and 152, a disk controller 154, 10 and an FVR controller 156, typically based on an Intel 86/05 board. The output of the FVR controller 156 is supplied to the FVR vector to raster converter 126 via an interface 157 and a SBX bus.

The vector to raster converter FVR 126 (Fig. 4) 15 comprises a graphic processor 158, a basic form memory and depth shifter 160, a synchronizer 162, diagnostic circuitry 163, and three slice memories 164, 166 and 168 coupled together, and also coupled to the basic form memory and depth shifter 160 by means of 20 a data bus 170, and an output buffer 169. The function and structure of these elements will be described hereinafter in detail.

The raster outputs from slice memories 164, 166 and 168 are supplied cyclically to output buffer 169, which 25 also receives an output from graphic processor 158. Output buffer 169 provides a video data output to a video interface circuit 172 forming part of the FCUB circuitry. The video interface circuit 172 is controlled by a FCUB processor 180, via a multibus 174. The 30 processor 180 also controls a correction memory 176 and a grid simulator 178. FCUB processor, which is typically an Intel 86/05, communicates with the FPU via an RS 232 port. Video interface 172 provides suitable output for operation of the IFUB circuitry 130.

Reference is now made to Fig. 6 which illustrates the 35 vector to raster conversion circuitry in conceptual block diagram form so as to facilitate understanding of its function.

As noted above in connection with Fig. 5, the vector 40 to raster converter comprises an FVR controller 156 which operates the functional blocks of Fig. 6 via a graphic processor 158. Graphic processor 158 receives layout information from the FPU 120 (Fig. 4) in vector format, typically in slices of width of 32 pixels 45 and length of up to 48,000 pixels. The graphic processor converts the vector information into a collection of coordinates and basic form selection instructions which indicate the path of the desired vector, in accordance with a modified version of the 50 Brezenheim algorithm is explained, for example, in W.M. Newman and R.F. Sproull, Principles of Interactive Computer Graphics, Chapter 2, McGraw Hill, 1979.

Graphic processor 158 is operative to provide a 55 basic form selection instruction to basic form memory 160, which typically comprises a collection of E-Proms of 1.0 Megabit capacity, and which stores, in compressed raster format, the basic forms, typically circular elements and transverse slices thereof, which are the constituent elements of all basic artwork 60 patterns.

Basic form memory 160 preferably stores all of the 65 information regarding the stored collection of basic forms in a form indicated in Fig. 7. Each basic form is described by an array of vertical lines. Thus the shape, size and location

plane defined by the graphic processor is defined by the quantity y, which defines a baseline, the quantity delta y which indicates the height above the baseline at which each given vertical line begins, the quantity z,

70 which indicates the length of each vertical line, the quantity x, which defines the location in the x dimension at which the first vertical line appears and the quantity r which indicates how many times a given line configuration is repeated.

75 It is appreciated that layout patterns of size greater than the largest element stored in the basic form memory 160 can be formed out of a plurality of stored elements.

The graphic processor 158 also provides an output 80 representing the quantity x to the slice memory, which is in fact a collection of three memories each 32 x 64,000 pixel memories operating cyclically.

In response to the output of the graphic processor 158, the basic form library outputs one or typically a 85 series of elements to depth shifter 162, which is typically a P-ROM. More precisely, for each element, the basic form library outputs a 5 bit signal delta y to an adder 180 which also receives an output representing the quantity y from the graphic processor.

90 The principal output from the basic form library to the depth shifter 162 includes a 5 bit stream indicating the length of each vertical line and a 5 bit stream indicating r, the amount of times that the identical vertical line is repeated. The summed output y + delta

95 y from adder 180 is supplied as a control signal to the depth shifter 162 for determining the orientation of the element along the y axis.

The depth shifter is operative to provide an output signal, typically in 64 bit parallel form, of the basic 100 form in its desired y orientation in the image plane defined by the graphic processor. This output is received by two slice memories in tandem, the x input from the graphic processor to the slice memories determining the x orientation of the element in the 105 image plane defined by the graphic processor.

The graphic processor 158 also provides a color selection output to slice memories 164-168. By selecting the color, it effectively determines whether a write or erase function on a given basic form is performed.

110 The slice memories 164-168 output, one by one to output buffer 169 (Fig. 4).

It is a particular feature of the present invention that as described hereinabove there is provided a method for transferring vector information in the form of lines 115 and pads into raster format, the method comprising the steps of defining a line in the form of a translated basic form in an image plane and defining a pad in the form of a collection of basic forms. This method can be visualized by considering Fig. 8 which shows a line

120 defined by translated basic forms 178 and 172, each described by a collection of vertical lines. As seen in Fig. 8, the definition of a vector via a translated basic form includes the step of defining a linear translation of the basic form.

125 Fig. 9 illustrates a sliced vector defined by a translated basic form, and incorporating two portions, a top portion 174 and a bottom portion 176. It will be appreciated by persons skilled in the art that the present invention is not limited to what has

described hereinabove.

Rather the scope of the present invention is defined only by the claims which follow:

CLAIMS

1. An integrated artwork editing, archiving and production system comprising
 - means for editing and electronically archiving printed circuit design information in vector format;
 - means for receiving the archived printed circuit designs in vector format and converting the vector format to raster format in real time; and
 - means for laser writing the printed circuit designs in raster format directly onto a substrate.
2. An integrated artwork editing, archiving and production system according to claim 1 and wherein said substrate constitutes the artwork or mask which is used to expose the production panel.
3. An integrated artwork editing, archiving and production system according to claim 1 and wherein said editing and archiving means comprises a data handling unit and an archive unit and said raster conversion and writing means are embodied in a fabrication unit, all of the units being interconnected via a local area network.
4. An integrated artwork editing, archiving and production system according to claim 1 and wherein said means for converting the designs in vector format to raster format comprises:
 - a central processing unit receiving vector inputs from the archiving unit and being operative to indicate a desired pattern to be written;
 - basic form memory means operative to store in raster form basic forms of desired size and shape;
 - a graphic processor operative to receive an input from the central processing unit and to provide an output which enables the desired pattern to be defined from the basic forms, the output being operative to provide instructions to the basic form memory for selecting one or more desired basic forms and x and y coordinate information to determine the position of the one or more basic forms in two dimensional space;
 - depth shifter means operative to receive the output of the basic forms memory and an output from the graphic processor and to position the y coordinate location of the basic forms in accordance with the y coordinate information provided by the graphic processor; and
 - memory means receiving the output from the depth shifter in accordance with the x coordinate output from the graphic processor.
5. An integrated artwork editing, archiving and production system according to claim 4 and wherein said form memory means is operative to store a plurality of circular forms of different sizes.
6. An integrated artwork editing, archiving and production system according to claim 4 and wherein said memory means comprises a slice memory having three portions which operate cyclically.
7. A method for transferring vector information in the form of lines and pads into raster format, comprising the steps of defining a line in the form of a translated basic form in an image plane and defining a pad in the form of a collection of basic forms.
8. A method according to claim 7 and also comprising the step of dividing wide lines or large
9. A method according to either of claims 7 and 8 and wherein the step of defining the line in the form of a translated basic form includes the step of defining a linear translation of the basic form.
10. Apparatus for transferring vector information in the form of lines and pads into raster format comprising means for defining a line in the form of a translated basic form in an image plane and means for defining a pad in the form of a collection of basic forms.
11. Apparatus according to claim 10 and also comprising means for dividing wide lines or large pads into slices.
12. Apparatus according to either of claims 10 and 11 and wherein said means for defining the line in the form of a translated basic form includes means for defining a linear translation of the basic form.
13. Apparatus substantially as shown and described hereinabove.
14. Apparatus substantially as illustrated in any of the drawings.
15. A method substantially as shown and described hereinabove.

Printed in the United Kingdom for Her Majesty's Stationery Office, 8818935, 9/86 18996. Published at the Patent Office, 25 Southampton Buildings, London WC2A 1AY, from which copies may be obtained.

